

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

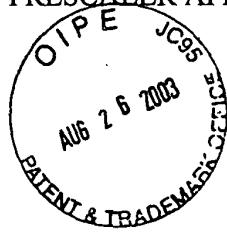
Applicant: Kevin W. Glass

Title: FREQUENCY PRESCALER APPARATUS, METHOD, AND SYSTEM

Docket No.: 80107.022US1

Filed: June 27, 2003

Examiner: Unknown



Serial No.: 10/608051

Due Date: N/A

Group Art Unit: Unknown

Commissioner for Patents
P.O.Box 1450
Alexandria, VA 22313-1450

We are transmitting herewith the following attached items (as indicated with an "X"):

☒ A return postcard.

☒ An Information Disclosure Statement (1 pg.), Form 1449 (2 pgs.), and copies of 27 cited documents.

If not provided for in a separate paper filed herewith, Please consider this a **PETITION FOR EXTENSION OF TIME** for sufficient number of months to enter these papers and please charge any additional fees or credit overpayment to Deposit Account No. 50-2359 .

LeMoine Patent Services, PLLC
c/o PortfolioIP
P.O. Box 52050
Minneapolis, MN 55402
952-473-8800

By: Dana B. LeMoine
Atty: Dana LeMoine
Reg. No. 40,062

CERTIFICATE UNDER 37 CFR 1.8: The undersigned hereby certifies that this correspondence is being deposited with the United States Postal Service with sufficient postage as first class mail, in an envelope addressed to: Commissioner for Patents, P.O.Box 1450, Alexandria, VA 22313-1450, on this 21st day of August, 2003.

Andrew J. Kurl
Name

[Signature]
Signature

(GENERAL)

S/N 10/608051

PATENT

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant: Kevin W. Glass

Examiner: Unknown

Serial No.: 10/608051

Group Art Unit: Unknown

Filed: June 27, 2003

Docket: 80107.022US1

Title: FREQUENCY PRESCALER APPARATUS, METHOD, AND SYSTEM

INFORMATION DISCLOSURE STATEMENT

Assistant Commissioner for Patents

P.O.Box 1450

Alexandria, VA 22313-1450

In compliance with the duty imposed by 37 C.F.R. § 1.56, and in accordance with 37 C.F.R. §§ 1.97 *et. seq.*, the enclosed materials are brought to the attention of the Examiner for consideration in connection with the above-identified patent application. Applicant respectfully requests that this Information Disclosure Statement be entered and the documents listed on the attached Form 1449 be considered by the Examiner and made of record. Pursuant to the provisions of MPEP 609, Applicant requests that a copy of the 1449 form, initialed as being considered by the Examiner, be returned to the Applicant with the next official communication.

Pursuant to 37 C.F.R. §1.97(b), it is believed that no fee or statement is required with the Information Disclosure Statement. However, if an Office Action on the merits has been mailed, the Commissioner is hereby authorized to charge the required fees to Deposit Account No. 50-2359 in order to have this Information Disclosure Statement considered.

The Examiner is invited to contact the Applicant's Representative at the below-listed telephone number if there are any questions regarding this communication.

Respectfully submitted,

KEVIN W. GLASS

By his Representatives,
LeMoine Patent Services, PLLC
c/o PortfolioIP
P.O. Box 52050
Minneapolis, MN 55402
952-473-8800

Date August 21, 2003

By Dana B. LeMoine
Dana LeMoine
Reg. No. 40,062

CERTIFICATE UNDER 37 CFR 1.8: The undersigned hereby certifies that this correspondence is being deposited with the United States Postal Service with sufficient postage as first class mail, in an envelope addressed to: Commissioner of Patents, P.O.Box 1450, Alexandria, VA 22313-1450, on this 21st day of August, 2003

Andrew J. Kaul
Name

[Signature]
Signature

Substitute for form 1449A/PTO
**INFORMATION DISCLOSURE
STATEMENT BY APPLICANT**
(Use as many sheets as necessary)

Complete if Known

Applicant Number 10/608051
Filing Date June 27, 2003
First Named Inventor Glass, Kevin
Group Art Unit Unknown
Examiner Name Unknown

Attorney Docket No: 80107.022US1

US PATENT DOCUMENTS						
Examiner Initial *	USP Document Number	Publication Date	Name of Patentee or Applicant of cited Document	Class	Subclass	Filing Date If Appropriate

FOREIGN PATENT DOCUMENTS						
Examiner Initials*	Foreign Document No	Publication Date	Name of Patentee or Applicant of cited Document	Class	Subclass	T ²

OTHER DOCUMENTS -- NON PATENT LITERATURE DOCUMENTS						
Examiner Initials*	Cite No ¹	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published.				T ²
		CHAE, KWAN-YEOB, et al., "Double Precharge TSPC for High-Speed Dual Modulus Prescaler", <u>IEEE</u> , (1999), pp. 609-612				
		CHANG, W-H, et al., "A Low-Power and Low-Noise CMOS Prescaler for 900 MHz to 1.9 GHz Wireless Applications", <u>IEEE 1999 Custom Integrated Circuits Conference</u> , (1999), pp. 597-600				
		CHI, BAOYONG, et al., "2/3 Divider Cell Using Phase Switching Technique", <u>Electronics Letters</u> , Volume 37, (July 2001), pp. 875-877				
		DE MUER, BRAM, et al., "A CMOS Monolithic $\Delta \Sigma$ -Controlled Fractional-N Frequency Synthesizer for DCS-1800", <u>IEEE Journal of Solid-State Circuits</u> , Volume 37, (July 2002), pp. 835-844				
		DULGER, FIKRET, et al., "Design Considerations in a BiCMOS Dual-Modulus Prescaler", <u>2002 IEEE Radio Frequency Integrated Circuits Symposium</u> , (2002), pp. 177-180				
		HSU, JUNE-MING, et al., "Low-Voltage CMOS Frequency Synthesizer for ERMES Pager Application", <u>IEEE Transactions on Circuits and Systems - II: Analog and Digital Signal Processing</u> , Volume 48, (2001), pp. 826-834				
		HUNG, CHIH-MING, et al., "A Fully Integrated 1.5-V 5.5-GHz CMOS Phase-Locked Loop", <u>IEEE Journal of Solid-State Circuits</u> , Volume 37, (April 2002), pp. 521-525				
		HUNG, CHIH-MING, et al., "Fully Integrated 5.35-GHz CMOS VCOs and Prescalers", <u>IEEE Transactions on Microwave Theory and Techniques</u> , Volume 49, (January 2001), pp. 17-22				
		KNAPP, HERBERT, et al., "2-GHz/2-mW and 12-GHz/30-mW Dual Modulus Prescalers in Silicon Bipolar Technology", <u>IEEE Journal of Solid-State Circuits</u> , Volume 36, (September 2001), pp. 1420-1423				
		KNAPP, HERBERT, et al., "36 GHz Dual-Modulus Prescaler in SiGe Bipolar Technology", <u>2002 IEEE Radio Frequency Integrated Circuits Symposium</u> , (2002), pp. 239-242				
		LAM, FLEMING, et al., "5+ GHz CMOS Prescaler", <u>2001 IEEE International SOI Conference</u> , (2001), pp. 65-66				
		LEE, KANG-YOON, et al., "Full-CMOS 2.4GHz Wideband CDMA Transmitter and Receiver with Direct Conversion Mixers and DC-Offset Cancellation", <u>2001 Symposium on VLSI Circuits Digest of Technical Papers</u> , (2001), pp. 7-10				

DATE CONSIDERED

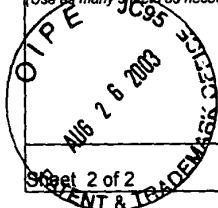
EXAMINER

Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it contains a valid OMB control number.

Substitute for form 1449A/PTO

**INFORMATION DISCLOSURE
STATEMENT BY APPLICANT**

(Use as many sheets as necessary)



Sheet 2 of 2

Complete if Known

Application Number	10/608051
Filing Date	June 27, 2003
First Named Inventor	Glass, Kevin
Group Art Unit	Unknown
Examiner Name	Unknown

Attorney Docket No: 80107.022US1

OTHER DOCUMENTS -- NON PATENT LITERATURE DOCUMENTS

Examiner Initials*	Cite No. ¹	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published.	T ²
		MALIGEORGOS, JAMES P., et al., "A Low-Voltage 5.1-5.8-GHz Image-Reject Receiver with Wide Dynamic Range", <u>IEEE Journal of Solid-State Circuits</u>, Volume 35, (December 2000), pp. 1917-1926	
		OHIRA, TAKASHI, et al., "An X-Band GaAs Monolithic Voltage Controlled Frequency Divider with Ultra-Low DC Power Consumption", <u>Proceedings of APMC</u>, (2001), pp. 127-130	
		PRETL, HARALD, et al., "A W-CDMA Zero-IF Front-End for UMTS in a 75 GHz SiGe BiCMOS Technology", <u>2001 IEEE Radio Frequency Integrated Circuits Symposium</u>, (2001), pp. 9-12	
		SOARES, JR., J N., et al., "A 1.6-GHz Dual Modulus Prescaler Using the Extended True-Single-Phase-Clock CMOS Circuit Technique (E-TSPC)", <u>IEEE Journal of Solid-State Circuits</u>, Volume 34, (January 1999), pp. 97-102	
		SOARES, JR., JOAO N., et al., "The Use of Extended TSPC CMOS Structures to Build Circuits with Doubled Input/Output Data Throughput", <u>IEEE</u>, (2000), pp. 228-233	
		SUNG, KI-HYUK, et al., "Comments on 'New Dynamic Flip-Flops for High-Speed Dual-Modulus Prescaler'", <u>IEEE Transactions on Solid-State Circuits</u>, Volume 35, (June 2000), pp. 919-920	
		THIBOUT, MARC, "A 480µW 2GHZ Ultra Low Power Dual-Modulus Prescaler in 0.25µM Standard CMOS", <u>IEEE International Symposium on Circuits and Systems</u>, (May 2000), pp. 741-744	
		TOURNIER, ERIC, et al., "A 14.5 GHz-0.35µm Frequency Divider for Dual-Modulus Prescaler", <u>2002 IEEE Radio Frequency Integrated Circuits Symposium</u>, (2002), pp. 227-230	
		WASSATSCH, ANDREAS, et al., "Scalable Counter Architecture for a Pre-loadable 1GHz@0.6µm/5V Prescaler in TSPC", <u>IEEE</u>, (2001), pp. 92-95	
		WU, PING, et al., "A CMOS Triple-band Fractional-N Frequency Synthesizer for GSM/GPRS/EDGE Applications", <u>IEEE</u>, (2001), pp. 706-709	
		YAN, HONGYAN, et al., "A High-Speed CMOS Dual-Phase Dynamic-Pseudo NMOS ((DP)²) Latch and Its Application in a Dual-Modulus Prescaler", <u>IEEE Journal of Solid-State Circuits</u>, Volume 34, (October 1999), pp. 1400-1404	
		YUAN, J-R, et al., "Fast CMOS Nonbinary Divider and Counter", <u>Electronics Letters</u>, Volume 29, (June 1993), pp. 1222-1223	
		YUAN, J-R, et al., "New Domino Logic Precharged by Clock and Data", <u>Electronics Letters</u>, Volume 29, (December 1993), pp. 2188-2189	
		YUAN, JIREN, et al., "Pushing the Limits of Standard CMOS", <u>IEEE Spectrum</u>, (February 1991), pp. 52-53	
		YUN, WONJOO, et al., "New High Speed Dynamic D-Type Flip Flop For Prescaler", <u>ISIE 2001</u>, (2001), pp. 629-631	

EXAMINER

DATE CONSIDERED

Substitute Disclosure Statement Form (PTO-1449)

* EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant. ¹ Applicant's unique citation designation number (optional) ² Applicant is to place a check mark here if English language Translation is attached